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## AMENDMENT TO THE CLAIMS

The listing of the claims will replace all prior versions and listings of claims in the application:

## LISTING OF CLAIMS

Please cancel claims 3 and 19 without prejudice.

Please amend the claims as follows:

1    1. (Currently Amended)     A memory driver comprising:

2         selection logic, to receive an address for promotion to a memory, and to provide an

3    indication of whether to promote the received address or a modified version thereof to the

4    memory;

5         a multiplexing element, responsive to the selection logic, to selectively promote either the

6    received address or the modified version thereof to the memory based, at least in part, on the

7    received indication;~~and~~

8         a pulse generator element, to receive a clock signal and produce at least two reference

9    signals, overlapping yet offset from one another in time; and

10        one or more driver elements, coupled to the multiplexing element and responsive to the

11    pulse generator element, to receive content promoted from the multiplexing element during a

12    precharge phase the reference signals, and to assert the content received from the multiplexer to

13    the memory during a discharge phase of the reference signals.


1    2. (Previously Amended)     A memory driver according to claim 1, further comprising:

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2        a latch element including the pulse generator and driver element(s), coupled to the

3    multiplexing element, to assert address content received from the multiplexing element to the

4    memory.


1    3. (Cancelled) A memory driver according to claim 2, the latch element comprising:

2        a pulse generator element, to receive a clock signal and produce at least two reference

3    signals, overlapping yet offset from one another in time; and

4    one or more driver elements, coupled to the multiplexing element and responsive to the pulse

5    generator element, to receive content promoted from the multiplexing element during a

6    precharge phase the reference signals, and to assert the content received from the multiplexer to

7    the memory during a discharge phase of the reference signals.


1    4. (Previously Amended)    A memory driver according to claim 2, the pulse generator element

2    comprising:

3        two parallel processing paths, one of which including a delay element, wherein the

4    parallel processing paths receive the clocking signal, or a delayed version thereof, at a gate of a

5    transistor to control the precharge and discharge cycles of the coupled latch.


1    5. (Previously Amended)    A memory driver according to claim 2, the driver element

2    comprising:

3        a differential domino transistor architecture, coupled to the multiplexer output and

4    responsive to the pulse generator, to generate a differential memory output of an element of the

5    promoted address content and its complement.


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1    6. (Original)   A memory driver according to claim 1, the selection logic comprising:

2        detection logic, to determine whether at least a subset of the received address is

3    composed of zeroes.


1    7. (Original)   A memory driver according to claim 6, wherein the detection logic is a one-detect

2    circuit.


1    8. (Original)   A memory driver according to claim 1, the selection logic comprising:

2        detection logic, to determine whether at least a subset of the received address is

3    composed of a predefined value.


1    9. (Original)   A memory driver according to claim 1, the multiplexer element comprising:

2        a first and second set of stacked transistors, wherein individual transistors of the first set

3    are coupled to receive at their gate one of an indication from the selection logic, an address, and

4    a process identification (PID) value, while individual transistors of the second set are coupled to

5    receive at their gate a complement of the indication, the address and the PID value.


1    10. (Original)  A memory driver according to claim 9, wherein depending on the indication

2    received from the selection logic, the multiplexer element promotes either the received address

3    and complement thereof, or the process identifier (PID) and complement thereof to the latch

4    element.


1    11. (Previously Amended)    A memory driver according to claim 2, the latch comprising:


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2        a first and second differential set of transistors, coupled to the multiplexing element, to

3    assert either the received address and complement thereof, or the PID and complement thereof to

4    a memory device.


1    12. (Original) A memory driver according to claim 11, wherein the latch is coupled to the

2    multiplexing element through a transistor responsive to a pulse generator, such that the latch is

3    isolated from the multiplexing element during a precharge phase of the pulse generator, and

4    asserts content at the output of the multiplexing element during a discharge phase of the pulse

5    generator.


1    13. (Previously Withdrawn)  A system comprising:

2        a content addressable memory (CAM); and

3        a memory driver, coupled with the CAM, to receive an address for assertion to the CAM,

4    and to selectively modify the at least a subset of the received address to reflect a process

5    identifier based, at least in part, on at least a subset of content of the received address.


1    14. (Previously Withdrawn)  A system according to claim 13, the memory driver comprising:

2        selection logic, to receive the address for promotion to a CAM cell, and to provide an

3    indication of whether to promote the received address or a modified version thereof to the CAM

4    cell; and

5        a multiplexing element, responsive to the selection logic, to selectively promote either the

6    received address or the modified version thereof to the CAM cell based, at least in part, on the

7    received indication.

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1    15. (Previously Withdrawn)   A system according to claim 14, the memory driver further

2    comprising:

1        a latch element, coupled to the multiplexing element, to assert address content received

2    from the multiplexing element to the memory cell.


1    16. (Original)  A method implemented within a memory driver comprising:

2        receiving at least a subset of an address for promotion to a memory; and

3        selectively replacing at least the subset of the received address with a process identifier

4    (PID) if it is determined that the subset of the received addresses is composed of zeroes.


1    17. (Original)  A method implemented within a memory driver according to claim 16, further

2    comprising:

3        analyzing the received subset of the address to determine whether the subset of composed

4    of zeroes and, if so, to provide an indication to a multiplexing element to replace the received

5    subset of the address with the process identifier.


1    18. (Original)  A method implemented within a memory driver according to claim ~~18~~ 17, further

2    comprising:

3        asserting either the received address, or a modified version thereof based, at least in part,

4    on whether the received subset of the address is composed of zeroes.


1    19. (Cancelled)        A storage medium comprising content, which when executed by an

2    accessing machine, causes the machine to implement a method according to claim 16.


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1    20. (Original)  A storage medium comprising content which, when executed by an accessing

2    machine, causes the machine to generate a memory driver according to claim 1.